Data processing system with virtual memory addressing and memory access controlled by keys.

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Abstract

Independent key memory control unit (KMU) coupled to the address conversion unit (ACU) of the processor (PIU), with a key memory (KM) driven via real memory addresses, the key memory containing entries (KEY) for each section of data, e.g. a page, separately protected in the main memory. Each entry consists of the memory key (ACC) and three further control bits (F, R and C), of which the last also serves for administration. Driving of the address conversion unit (ACU) and processor (PIU) via common switchable input interface (KMIA), while the input/output processors (IOP) are coupled via a separate interface. The key memory control unit (KMU) works under command control. For the purposes of address conversion, it is driven by the address conversion unit (ACU) at each memory request of the processor (PIU), if the administration bits are to be altered or if there is still no entry in the address conversion buffer (TLB). Characterisation of entries in the address conversion buffer (TLB) in a memory (KIAT), addressable in parallel with the key memory and of the same depth, prevents unnecessary testing of the address conversion buffer (TLB) when entries are to be cleared.